WHAT IS CLAIMED IS:

1. A method for communicating a multiple-word digital message with an isochronous-signal processor, said method comprising:

receiving a request to transfer a multiple-word block of data;

acknowledging said request;

serially transferring said block of data over multiple frames without interrupting isochronous data flow; and

compiling said block of data in a data buffer.

2. The method of claim 1, wherein each word of said block of data is transferred in a different frame.

3. The method of claim 1, wherein said isochronous-signal processor functions as an audio codec slave, and said communicating is with a digital controller via an audio codec-link.

4. The method of claim 1, wherein said block of data is transferred in non-consecutive frames.

5. The method of claim 1, wherein said transferring is said isochronous-signal processor receiving said block of data.

6. The method of claim 5, wherein said compiling is performed as said each word is received.

7. The method of claim 5, further comprising receiving a total word count value with said transfer request, and further comprising verifying a number of words received with said word count value.

8. The method of claim 5, further comprising processing said block of data after said compiling is complete.

9. The method of claim 8, further comprising acknowledging said processing of said block of data after said processing is complete.

10. The method of claim 1, wherein said transferring is said isochronous-signal processor sending said block of data.

11. The method of claim 10, wherein said compiling of said block of data is performed before said transfer of said data, and said method further comprising acknowledging that said block of data is ready to transfer after said compiling.

12. The method of claim 10, further comprising said isochronous-signal processor generating a total word count value, and further comprising verifying a number of words sent with said word count value.

13. An isochronous-signal processor for processing isochronous signals, said processor comprising:

a digital interface providing a serial digital link to a digital controller, wherein said isochronous signals are transferred over said digital link;

a set of registers for transferring a non-isochronous multiple-word block of data over said digital link, said register set comprising

a control register;

a status register; and

a data register; and

a data buffer for storing said multiple-word block of data, wherein said data buffer is separate from said set of registers.

14. The processor of claim 13, further comprising:

an analog mixer for processing said isochronous signals in analog format;

at least one digital to analog converter (DAC) coupled between said digital interface and said analog mixer; and

at least one analog to digital converter (ADC) coupled between said analog mixer and said digital interface;

15. The processor of claim 13, wherein said control register stores information for controlling said multiple-word transfer, said status register stores information for monitoring a status of said multiple-word transfer, and each word of said block of data is sequentially transferred through said data register during said multiple-word transfer.

16. The processor of claim 13, wherein said isochronous signals represent audio information.

17. The processor of claim 16, wherein said serial digital link is an audio codec-link.

18. The processor of claim 13, wherein said processor is implemented on one or more devices selected from the group consisting of: an audio codec integrated circuit, a digital signal processor (DSP) integrated circuit, and a combination thereof.

19. The processor of claim 13, wherein said control and status registers are logical registers sharing a single physical register address.

20. The processor of claim 13, wherein said data buffer comprises a command buffer for storing a block of data received over said digital link, and a status buffer for storing a block of data to send over said digital link.

21. The processor of claim 13, further comprising a mechanism for determining the end of said multiple-word block of data.

22. The processor of claim 13, wherein said mechanism is a word counter.

23. A protocol for transferring a multiple-word block of data between an isochronous-signal processor and a digital controller over a serial digital interface, said protocol comprising:

said digital controller sending a request to said isochronous-signal processor to transfer said multiple-word block of data, wherein said block of data is non-isochronous;

said isochronous-signal processor acknowledging said request;

serially transferring said block of data over multiple frames without interrupting isochronous data flow; and

said isochronous-signal processor compiling said block of data in a data buffer.

24. The protocol of claim 23, wherein each word of said block of data is transferred in a different frame.

25. The protocol of claim 23, wherein said block of data is transferred in non-consecutive frames.

26. The protocol of claim 23, wherein said block of data is transferred in consecutive frames.